DETAILED ACTION

1. The amendment filed on 06/19/2007 has been entered. Claims 1,2,4-9,17-19 and 21-29 are pending for further examination.

2. Claims 2,5-9,21 and 22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 21, it is unclear whether "a new format", line 3, is a format that is different from "a format" recited in claim 1.

As per claim 22, "said fast loading", line 4, lacks a proper antecedent basis.

As per claim 2, Since it is in definite as to what is considered "a normal slow floating point loading instruction", "a deviation from a normal slow floating point loading instruction", line 4, is also indefinite as to what it is. Further, "storage", line 3, should be -- memory --.

As per claim 24, "said processing unit" should be -- said co-processing unit --.

3. Claims 17-19 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Lao et al. (7,031,994).

As per claims 17, Lao et al discloses matrix operation on matrix data stored in a standard format in the memory, including (step 1, see col. 9, lines 28-50) separating the matrix (A) into blocks, rearrange and placing in the memory said block by reading each block in row-wise to the workspace sequentially, then writing back in column-wise into their original spots in the

memory. The separation of matrix and rearrangement of blocks (step 1) clearly result in a matrix (A1) having blocks of data to be contiguous blocks of contiguous data stored in the memory in a nonstandard format that permits said matrix data (A1) to be moved from said storage memory system into a position for performing said matrix operation (matrix transpose) more quickly than if said matrix data had been moved as stored in said standard format as claimed. Further, Lao similarly discloses in Col. 16 matrix operation including separating a matrix (A) into blocks of size 2-by-2 (Col. 16, lines 27-35); rearrange and storing the blocks of data (Col. 16, lines 35-45) into contiguous blocks of contiguous data (col.16, lines 43-35) in a nonstandard format in which the blocks occupy a position different from its original position while maintaining an original data content within each block as claimed.

As per claims 18 and 19, Lao also discloses in Col. 16, line 37-58, repetitively loading the blocks using 2x2 crisscrossing technique to form a transpose data (AT) of the matrix (A).

4. Claims 23, 26 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lao et al. (7,031,994) in view of Gulley et al (5,025,407).

As per claims 23 and 26 Lao et al discloses in figure 6 an apparatus having a processor (600), a memory system (602) and a plurality of data register (202,604), for perform matrix operation on matrix data stored in a standard format in the memory, including (step 1, see col. 9, lines 28-50) separating the matrix (A) into blocks, rearrange and placing in the memory said block by reading each block in row-wise to the workspace sequentially, then writing back in column-wise into their original spots in the memory. The separation of matrix and rearrangement of blocks (step 1) clearly result in a matrix (A1, col. 9, lines 47-50) having blocks

of data to be contiguous blocks of contiguous data in the memory such that said matrix data is represented in a nonstandard format that permits said matrix data (A1) to be moved from said storage memory system into a position for performing said matrix operation (matrix transpose) more quickly than if said matrix data had been moved as stored in said standard format as claimed. Further, Lao similarly discloses in Col. 16 matrix separation including separating a matrix (A) into blocks of size 2-by-2 (Col. 16, lines 27-35); rearrange and storing the blocks of data into contiguous blocks of contiguous data (col.16, lines 35-45) in a nonstandard format in which the blocks occupy a position different from its original position while maintaining an original data content within each block as claimed. It is noted that Lao et al. does not specifically disclose co-processor unit. However, Gulley et al. discloses in figure 2 a floating point co-processor (1200) having matrix capabilities in addition to a processor (200). It would have been obvious to a person of ordinary skill in the art to provide the apparatus of Lao et al. with a floating point coprocessor as taught by Gulley in order to increase the speed of processing.

As per claim 28, instructions that are processed the processor apparatus are seen as the claimed first software instructions to preliminarily process input data in a manner to generate a first error relative, and instructions that loads data to the co-processing unit for matrix are seen as the claimed second software instructions to subsequently process said input data in a manner to generate a correcting error.

5. Claims 24,25,27 and 29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. Claims 1 and 4 are allowed.

7. Applicant's arguments filed on 02/28/2008 and 03/19/2008 have been fully considered but they are not persuasive regarding claims 17-19, 23,26 and 28.

Regarding claims 17-19, it is respectfully submitted that Lao does discloses in Col. 16 matrix separation including separating a matrix (A) into blocks of size 2-by-2 (Col. 16, lines 27-35); rearrange and storing the blocks of data into contiguous blocks of contiguous data (col.16, lines 35-45) in a nonstandard format in which the blocks occupy a position different from its original position while maintaining an original data content within each block as claimed.

Regarding claims 23 and 26, the limitations "a loading of said matrix form said storage into said co-processing unit ..." that follows "permit", and "said matrix data to be place from said storage into said co-processing unit ..." that follows "allow", are not necessarily required by the claims.

Regarding claim 28, the claim does not specifically require that the new format to have the original content of data within the blocks is retained but the ordering of the blocks is changed.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong D. Ngo whose telephone number is (571) 272-3731. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lewis, Jr. A. Bullock can be reached on (571) 272-3759. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Chuong D Ngo/
Primary Examiner, Art Unit 2193

06/19/2008